ZKW
AF/S

Attorney's Docket No.: 42P17961 Patent

In re the Application of: Illikkal et al.
(inventor(s))

Application No.: 10/735,113

Filed: December 12, 2003

For: STRIPING ACROSS MULTIPLE CACHE LINES TO PREVENT FALSE SHARING
(title)

Mail Stop Appeal Brief – Patents
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SIR: Transmitted herewith is an **Appeal Brief** for the above-referenced application.

_____ Applicant claims small entity status. See 37 CFR 1.27.

__XX__ No additional claim fee is required.

The fee has been calculated as shown below:

	(Col. 1) Claims Remaining After Amd.		(Col. 2) Highest No. Previously Paid For	(Col. 3) Present Extra	SMALL ENTITY Rate	SMALL ENTITY Additional Fee	OTHER THAN A SMALL ENTITY Rate	OTHER THAN A SMALL ENTITY Additional Fee
Total Claims	* 16	Minus	** 20	0	X9	$	X18	$ 0
Indep. Claims	* 4	Minus	*** 4	0	X43	$	X86	$ 0
☐	**First Presentation of Multiple Dependent Claim(s)**				+145	$	+290	$
					Total Add. Fee	$	Total Add. Fee	$ 0

* If the entry in Col. 1 is less than the entry In Col. 2, write "0" in Col. 3.

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_____ Applicant(s) hereby Petition(s) for an Extension of Time of _____ month(s) pursuant to 37 C.F.R. § 1.136(a).

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Date: Sept. 15, 2006

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September 15, 2006	Yuko Tanaka	Y. Tanaka	Sept. 15, 2006
Date Mailed	Name	Signature	Date

Attorney Docket No.: 42P17961 *Patent*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Illikkal et al.	)	Examiner: Gu, Shawn X.
	)	
Application No.: 10/735,113	)	Art Unit: 2189
	)	
Filed: December 12, 2003	)	
	)	
For: STRIPING ACROSS MULTIPLE CACHE LINES TO PREVENT FALSE SHARING	)	
	)	

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APPEAL BRIEF (37 C.F.R. § 41.37)

Sir:

This appeal brief is submitted pursuant to the Notice of Appeal mailed July 21, 2006, for the above-captioned patent application. The Notice of Appeal was filed in response to the final Office Action mailed April 25, 2006, and the Advisory Action mailed June 28, 2006. Applicants respectfully request consideration of this appeal and allowance of the application by the Board of Patent Appeals and Interferences.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Intel Corporation ("Intel"), a Delaware corporation having a principal place of business at 2200 Mission College Blvd., Santa Clara, California, 95052. Intel is the assignee of the entire right, title and interest in the above-captioned application by virtue of an assignment recorded at the U.S. Patent Office at Reel 014795, Frame 0433.

II. RELATED APPEALS AND INTERFERENCES

Appellants and Appellants' legal representative know of no interferences, appeals, or other proceedings that will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1, 2, 4-9, 11-13, 15-17, 19, and 20 are pending in the application and are the claims on appeal. All claims in the application currently stand rejected based on three references: U.S. Patent No. 6,912,602 B2 to Sano *et al.* (hereinafter "Sano"), excerpts from a book entitled, "Computer Architecture A Quantitative Approach, Second Edition" by Patterson et al., pages 431 to 438 (hereinafter "Patterson"), and U.S. Patent No. 6,389,468 B1 to Muller *et al.* (hereinafter "Muller"). The basis of rejection of the claims is as follows:

(i) Independent claims 1, 8, 12, and 16 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Sano in view of Patterson.

(ii) Dependent claims 2, 4, 6-7, 9, 11, 13, 15, 17, 19, and 20 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Sano in view of Patterson.

(iii) Dependent claim 5 stands rejected under 35 U.S.C § 103(a) as being unpatentable over Sano in view of Patterson, in further view of Muller.

In the Final Office Action mailed April 25, 2006, the Examiner further rejected claims 16, 17, 19, and 20 under 35 U.S.C. § 112, first paragraph, as failing to comply

with the written description requirement. However, the Examiner subsequently withdrew these § 112, first paragraph rejections in the Advisory Action mailed on June 28, 2006.

IV. STATUS OF AMENDMENTS

Prior to the final Office Action mailed April 25, 2006, claims 1, 2, 4-9, 11-13, 15-17, 19, and 20 were pending in the application. Applicants submitted a response to the final Office Action on June 13, 2006, but did not make any amendments to the pending claims, nor cancelled or added any claims. Therefore, all amendments made by Applicants in previous Office Actions have been entered by the Examiner, and the claims on appeal therefore incorporate all previous amendments.

A copy of all claims on appeal, as finally rejected by the Examiner on April 25, 2006, is attached hereto in Appendix A.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Embodiments of the present invention, as recited in the current independent claims 1, 8, 12, and 16, relate generally to a method, article of manufacture, or a computer system for striping a descriptor ring (e.g., see descriptor ring 304 in FIG. 4 of *Application*) to prevent false sharing of a cache line (e.g., see cache line 302 illustrated in FIG. 4 of *Application*) between a plurality of processors (e.g., see CPUs 0, 1, 2, and 3 illustrated in FIG. 4 of *Application*) of a computing system. Support can be found on page 8, lines 3-11 of the *Specification*.

In independent claims 1, 8, 12, and 16, the descriptor ring is striped according to a striping policy that assigns a first processor of the plurality of processors to a first descriptor according to the following relationship:

Processor Assignment = Descriptor_Position mod N,

where Descriptor_Position is a descriptor ring position of the first descriptor and N is a total number of the plurality of processors (e.g., see *Specification*, page 9, lines 5-15).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented in this appeal are:

(i) Whether independent claims 1, 8, 12, and 16 are obvious in view of Sano and Patterson.

(ii) Whether dependent claims 2, 9, 13, and 17 are obvious in view of Sano and Patterson.

(iii) Whether dependent claims 4-7, 11, 15, 19, and 20 are obvious in view of Sano and Patterson

VII. ARGUMENTS

This section sets forth Appellants' arguments against the rejections and in favor of the patentability of the claims on appeal. Part VII.A provides a brief overview of the Sano, Patterson, and Muller references, which the Examiner used to reject the claims on appeal. Part VII.B discusses why the combination of Sano and Patterson cannot render independent claims 1, 8, 12, and 16 obvious. Part VII.C discusses why the combination of Sano and Patterson cannot render dependent claims 2, 9, 13, and 17 obvious. Part VII.D discusses why the combination of Sano and Patterson cannot render dependent claims 4-7, 11, 15, 19, and 20 obvious.

A. Brief Overview of Sano, Patterson, and Muller

1. Sano

FIG. 1 of Sano discloses a system 10 for receiving packets from multiple interface circuits 20A-20C. System 10 includes multiple processors 12A-12N and a memory 24 linked to an interconnect 22. Interconnect 22 is linked to interface circuits 20A-20C via a packet DMA circuit 16 and a switch 18. FIG. 6 illustrates a descriptor ring 100 including multiple descriptors 0 to N-1. The descriptors within descriptor ring 100 are made available to packet DMA circuit 16 to store or read packets for transmission. See, e.g.,

Sano, col. 13, lines 42-67. Sano discloses that the descriptors 0 to N-1 are used in consecutive order. In fact, Sano expressly discloses

> The descriptors may be used in a ring. That is, descriptors may be used in **consecutive order** starting at descriptor 0 and proceed to descriptor N-1. When the last descriptor N-1 has been used, the next descriptor to be used is (*sic*) descriptor 0 (indicated in FIG. 6 by the dashed line from descriptor N-1 to descriptor 0).

Sano, col. 13, lines 53-58 (Emphasis added).

2. Patterson

The excerpts of Patterson cited by the Examiner disclose a technique for interleaving access to multiple memory banks. Patterson states, "the purpose of interleaved memory is to try to take advantage of the potential memory bandwidth of *all* the DRAMs in the system..." (*Patterson*, page 431, line 38 to page 432, line 1). Patterson further discloses that interleaving access to multiple memory banks in a multiprocessor system may help avoid memory bank conflicts (see, e.g., *Patterson*, page 435, section entitled, "Fourth Technique for Higher Bandwidth: Avoiding Memory Bank Conflicts"). Patterson discloses that interleaving the memory banks may be accomplished by "mapping of an address to a location in a memory bank" according to the following relations:

Bank number = Address MOD Number of banks

Address within bank = [Address/Number of banks]

See *Patterson*, page 436.

3. Muller

Muller discloses an apparatus capable of distributing the processing of network packets received at a multiprocessor computer system among the plurality of processors within the computer system. The Examiner cites Muller in reference to dependent claim

5, as merely disclosing a "computer system with descriptors where the descriptors are 16 bytes long and the cache line is 64 bytes in order to allow efficient transfer of 4 descriptors in one transfer cycle." *Office Action* mailed April 25, 2006, page 9, section 6.

B. The combination of Sano and Patterson do not render independent claims 1, 8, 12, and 16 obvious

The Examiner rejected independent claims 1, 8, 12, and 16 under 35 USC § 103(a) as being unpatentable over the combination of Sano and Patterson.

"To establish prima facie obviousness of a claimed invention, **all the claim limitations** must be taught or suggested by the prior art. All words in a claim must be considered in judging the patentability of that claim against the prior art." M.P.E.P. § 2143.03.

Independent claim 1 is nonobvious over Sano and Patterson for two independent reasons.

Independent Reason #1

First, independent claim 1 recites, in pertinent part

> placing the first descriptor in a descriptor ring according to a striping policy to prevent false sharing of a cache line between a plurality of processors...

Appellants respectfully submit that the combination of Sano and Patterson also fails to teach or suggest a striping policy to prevent false sharing of a cache line between a plurality of processors.

To be sure Sano discloses that descriptors 0 to N-1 within descriptor ring 100 (see FIG. 6 of Sano), are used in consecutive order. When the last descriptor N-1 has been used, the next descriptor to be used is descriptor 0, as indicated in FIG. 6 by the dashed line from descriptor N-1 to descriptor 0. Therefore, Sano does not disclose placing descriptors 0 to N-1 into descriptor ring 100 according to a striping policy to prevent false sharing of a cache line between processors 12A-12N. Rather, Sano discloses a consecutive ordering technique.

Furthermore, Sano fails to disclose, teach, or suggest any technique to prevent false sharing of a cache line between processors 12A-12N, much less using a striping policy on descriptor 100 to prevent false sharing. In affirmation of this, the Examiner acknowledged, "Sano does not teach that the first descriptor is placed in a descriptor ring according to a striping policy to prevent false sharing of the cache line between the plurality of processors of the computer system." *Office Action* mailed April 25, 2006, page 4.

To overcome this deficiency in Sano, the Examiner cites Patterson as teaching the missing elements. However Patterson merely discloses interleaving memory banks. Patterson fails to teach or suggest a striping policy to prevent false sharing of a cache line between a plurality of processors of a computer system. Similar to Sano, Patterson makes no reference to a striping policy to prevent false sharing of a cache line between multiple processors. At best, Patterson discloses that interleaving access to multiple memory banks in a multiprocessor system may help avoid memory bank conflicts. However, avoiding memory bank conflicts does not teach or suggest preventing false sharing of a cache line. The DRAM memory banks of Patterson have no relation to a cache line and interleaving access to the DRAM memory banks has no relation to preventing false sharing of a cache line.

Independent Reason #2

The second independent reason why claim 1 is nonobvious over Sano and Patterson relates to the following pertinent portion of claim 1,

> wherein the striping policy assigns a first processor of the plurality of processors to the first descriptor according the following relationship:
> Processor Assignment = Descriptor_Position mod N,
> where Descriptor_Position is a descriptor ring position of the first descriptor and N is a total number of the plurality of processors.

Appellants respectfully submit that the combination of Sano and Patterson fails to teach or suggest a striping policy that assigns a processor of a plurality of processors to a descriptor according to the above recited relationship where 'N' is the total number of the processors.

As discussed above, Sano fails to disclose, teach, or suggest any striping policy and certainly not the specific striping policy recited in independent claim 1. The

Examiner has acknowledged this in both Office Actions mailed January 17, 2006 and April 25, 2006, page 4. Therefore, the Examiner cites Patterson as teaching this missing element.

However, Patterson does not disclose, teach, or suggest a technique for assigning processors to descriptors. Rather, Patterson discloses a technique of interleaved memory including multiple memory banks where

> [t]he mapping of an address to a location in a memory bank can be expressed as two problems:
>
> Bank number = Address MOD **Number of banks**
>
> Address within bank = [Address/Number of banks]

Patterson, page 436 (Emphasis added). Accordingly, Patterson discloses a technique of mapping addresses to locations in memory banks—not how to assign processors to descriptors in a descriptor ring.

First, a "Bank number" is distinctly different than a "Processor Assignment". Second, Patterson fails to teach or suggest "mod N" where N is a number of processors. Rather Patterson discloses "mod Number of banks". A number of memory banks cannot reasonably be interpreted as teaching a number of processors. As such, the Examiner simply has failed to teach or suggest "Processor Assignment = Descriptor_Position mod N, where Descriptor_Position is a descriptor ring position of the first descriptor and N is a total number of the plurality of processors.

Finally, the Examiner himself has acknowledged "**[n]either of the cited references** specifically discloses that the first descriptor is assigned to a processor of the plurality of processors according to the relationship of Processor assignment = Descriptor_Postion mod N" (*Office Action* mailed April 25, 2006, page 6, lines 3-5). Since M.P.E.P. §2143.03 expressly requires that the prior art teach or suggest all limitation of a claim, by the Examiner own admission, the prior art of record does not establish a prima facie case of obviousness.

For at least the two independent reasons discussed above, the combination of Sano and Patterson fails to teach or suggest all elements of claim 1, as required under M.P.E.P. § 2143.03. **Independent claims 8, 12, and 16 include similar nonobvious elements as independent claim 1**. Accordingly, Appellants request that the instant §103(a) rejections of independent claims 1, 8, 12, and 16 be withdrawn.

C. The combination of Sano and Patterson do not render dependent claims 2, 9, 13, and 17 obvious

The Examiner rejected dependent claims 2, 9, 13, and 17 under 35 USC § 103(a) as being unpatentable over the combination of Sano and Patterson.

"To establish prima facie obviousness of a claimed invention, **all the claim limitations** must be taught or suggested by the prior art. All words in a claim must be considered in judging the patentability of that claim against the prior art." M.P.E.P. § 2143.03.

Dependent claim 2 recites,

> 2. The method of claim 1 wherein the striping policy comprises placing the first descriptor in the descriptor ring such that the first descriptor and a second descriptor in the descriptor ring do not share the cache line when the second descriptor is requested, wherein the first descriptor to be the next descriptor requested from the descriptor ring after the second descriptor.

Appellants respect submit that the combination of Sano and Patterson fails to disclose, teach, or suggest a striping policy that places a first descriptor in a descriptor ring such that the first descriptor and a second descriptor in the descriptor ring do not share a cache line when the second descriptor is requested. Note, claim 2 recites that the first descriptor is the next descriptor to be requested from the descriptor ring. In other words, the first and second descriptors are consecutive descriptors to be requested from the descriptor ring. Sano and Patterson simply make no mention of a striping policy that places a first and second descriptor into a descriptor ring so that the first and second descriptors do not share the cache line when the second descriptor is requested and the first and second descriptors are consecutively requested descriptors.

The Examiner cites Patterson as teaching claim 2 and references Figure 5.34 on page 437 of Patterson. However, Patterson makes not reference to descriptors or cache lines and Applicants respectfully submit that a memory bank is not equitable to a cache line nor is an address within a memory bank equitable to a descriptor. In any event, the cited references provide not motivation to make such a connection. Rather, it appears to Appellants that the Examiner has indulged in improper hindsight reasoning, based on

Appellants specification, to impermissibly rearrange and distort parts of two references in an attempt to meet the terms of claim 1. See, M.P.E.P. §2145(X)(A).

For the reasons discussed above, the combination of Sano and Patterson fails to teach or suggest all elements of dependent claim 2, as required under M.P.E.P. § 2143.03. **Dependent claims 9, 13, and 17 include similar nonobvious elements as dependent claim 2.** Dependent claims 2, 9, 13, and 17 are nonobvious over the prior art of record not only for the reasons discussed in this section VII.C, but also for the same reasons as discussed above in connection with their respective independent claims in section VII.B. Accordingly, Appellants respectfully request that the instant § 103 rejections of dependent claims 2, 9, 13, and 17 be withdrawn.

D. The combination of Sano, Patterson, and Muller do not render dependent claims 4-7, 11, 15, 19, and 20 obvious

As to dependent claims 4-7, 11, 15, 19, and 20, if an independent claim is allowable, then any claim depending therefrom is also allowable. *See, e.g.,* MPEP § 2143.03; *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). As discussed above, independent claims 1, 8, 12, and 16 are in condition for allowance. Appellants submit that claims 4-7, 11, 15, 19, and 20 are therefore allowable by virtue of their dependence on allowable independent claims, as well as by virtue of the features recited in the claims. Appellants respectfully request withdrawal of the rejections and allowance of these claims.

VIII. CONCLUSION

Given the above arguments supporting patentability, Appellants believes all claims on appeal are in condition for allowance. If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to allowance of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 292-8600.

Charge Deposit Account

Please charge our Deposit Account No. 02-2666 for any additional fee(s) that may be due in this matter, and please credit the same deposit account for any overpayment.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: Sept. 15, 2006

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APPENDIX A — CLAIMS

1. (Previously Presented) A method, comprising:

creating a first descriptor to correspond to a first data block; and

placing the first descriptor in a descriptor ring according to a striping policy to prevent false sharing of a cache line between a plurality of processors of a computer system, wherein the striping policy assigns a first processor of the plurality of processors to the first descriptor according the following relationship:

Processor Assignment = Descriptor_Position mod N,

where Descriptor_Position is a descriptor ring position of the first descriptor and N is a total number of the plurality of processors.

2. (Previously Presented) The method of claim 1 wherein the striping policy comprises placing the first descriptor in the descriptor ring such that the first descriptor and a second descriptor in the descriptor ring do not share the cache line when the second descriptor is requested, wherein the first descriptor to be the next descriptor requested from the descriptor ring after the second descriptor.

3. (Cancelled)

4. (Previously Presented) The method of claim 1 wherein the cache line is longer than the first descriptor.

5. (Original) The method of claim 4 wherein the cache line is 64 bytes long and the first descriptor is 16 bytes long.

6. (Previously Presented) The method of claim 1 further comprising receiving the first data block at an I/O device of the computer system from external to the computer system.

7. (Previously Presented) The method of claim 1 wherein the first data block is prepared at the computer system to be sent to an I/O device of the computer system.

8. (Previously Presented) An article of manufacture comprising:

a machine-readable medium including a plurality of instructions which when executed perform operations comprising:

allocating a first receive buffer at a computer system including a plurality of processors, the first receive buffer to store a first packet received at a network interface card (NIC) of the computer system;

creating a first descriptor corresponding to the first receive buffer; and

placing the first descriptor in a descriptor ring according to a striping policy to prevent false sharing between the plurality of processors of a cache line of the computer system, wherein the striping policy assigns a first processor of the plurality of processors to the first descriptor according the following relationship:

Processor Assignment = Descriptor_Position mod N,

where Descriptor_Position is a descriptor ring position of the first descriptor and N is a total number of the plurality of processors.

9. (Previously Presented) The article of manufacture of claim 8 wherein the striping policy comprises placing the first descriptor in the descriptor ring such that the first descriptor and a second descriptor in the descriptor ring do not share the cache line when the second descriptor is requested, the first descriptor to be the next descriptor requested from the descriptor ring after the second descriptor.

10. (Cancelled)

11. (Original) The article of manufacture of claim 8 wherein the plurality of instructions are embodied in a NIC device driver associated with the NIC.

12. (Previously Presented) The article of manufacture comprising:

a machine-readable medium including a plurality of instructions which when executed perform operations comprising:

creating a first descriptor at a computer system including a plurality of processors, the first descriptor to correspond to a first packet to be transmitted by a network interface card (NIC) of the computer system; and

placing the first descriptor in a descriptor ring according to a striping policy to prevent false sharing of a cache line between the plurality of processors of the computer system, wherein the striping policy assigns a first processor of the plurality of processors to the first descriptor according the following relationship:

Processor Assignment = Descriptor_Position mod N,

where Descriptor_Position is a descriptor ring position of the first descriptor and N is a total number of the plurality of processors.

13. (Original) The article of manufacture of claim 12 wherein the striping policy comprises placing the first descriptor in the descriptor ring wherein the first descriptor and a second descriptor in the descriptor ring to not share the cache line when the second descriptor is requested, the first descriptor to be the next descriptor requested from the descriptor ring after the second descriptor.

14. (Cancelled)

15. (Original) The article of manufacture of claim 12 wherein the plurality of instructions are embodied in a NIC device driver associated with the NIC.

16. (Previously Presented) A computer system, comprising:

a plurality of network interface cards (NICs);

a plurality of processors, each of the plurality of processors communicatively coupled to each of the plurality of NICs; and

a storage device operatively coupled to the plurality of processors, the storage device including a plurality of instructions which when executed by a processor of the plurality of processors perform operations comprising:

creating a first descriptor to correspond to a first packet; and

placing the first descriptor in a descriptor ring according to a striping policy to prevent false sharing of a cache line between the plurality of processors of the computer system, wherein the striping policy assigns a first processor of the plurality of processors to the first descriptor according the following relationship:

Processor Assignment = Descriptor_Position mod N,

where Descriptor_Position is a descriptor ring position of the first descriptor and N is a total number of the plurality of processors.

17. (Original) The computer system of claim 16 wherein the striping policy comprises placing the first descriptor in the descriptor ring wherein the first descriptor and a second descriptor in the descriptor ring to not share the cache line when the second descriptor is requested, the first descriptor to be the next descriptor requested from the descriptor ring after the second descriptor.

18. (Cancelled)

19. (Original) The computer system of claim 16 wherein execution of the plurality of instructions further perform operations comprising receiving the first packet at a NIC of the plurality of NICs.

20. (Original) The computer system of claim 16 wherein execution of the plurality of instructions further perform operations comprising preparing the first packet at the computer system, the first packet to be transmitted from a NIC of the plurality of NICs.

APPENDIX B— EVIDENCE

[No Evidence is Entered]

APPENDIX C — RELATED PROCEEDINGS

[No Related Proceedings]